IN THE CLAIMS

Claim 1 (currently amended): A method of reordering a scan chain for **[[the]]** design of testability on VLSI with low power dissipation, comprising ~~**the following steps of**~~:

(a) inputting scan chain register circuit data, including **[[the]]** **a** name of each register, **[[a]]** 2D coordinates, and power dissipation value(s);

(b) inputting **[[to]]** test pattern data on the scan chain;

(c) inputting conditions of **[[the]]** design specification **including** **[[: (1)]]** peak value of power dissipation at **[[the]]** **a** time of potential conversion of register; ~~**(2) the**~~ maximum of total connection length of **the** scan chain; and ~~**(3) the**~~ maximum of connection distance between ~~**adjacent**~~ two **adjacent** registers;

(d) determining whether a Feasible Solution meeting the maximum ~~**limit**~~ of **connection** distance between **the** two adjacent registers is provided;

(e) creating a database of the two adjacent registers;

(f) **if** an event ~~**impossibly**~~ meeting both the maximum **of the total connection length** ~~**limited distance**~~ and the maximum ~~**limited**~~ **of connection** distance, **[[and]]** the total length of the scan chain being ~~**deleted**~~ **ignored**;

(g) for **[[the]]** **a** given test pattern, re-ordering the registers on the scan chain for reduction of power dissipation, and ~~**it being determined**~~ whether **[[the]]** **determining** peak value limit of power dissipation and the ~~**limit condition of**~~ maximum **of** total **connection** length for the scan chain ~~**connection**~~ accord; and

(h) outputting **[[the]]** **an** updated scan chain arrangement and **[[the]]** **a** corresponding scan chain test pattern data**, wherein the event meeting the maximum of the total connection length of the scan chain is ignored in case of:**

(a) $L_{lim}<L^{min}$: no feasible solution given;

(b) $L^{min}<=L_{lim}<L^{max}$: at the time of the arrangement of the scan chain register at a next step, in addition to a search for a combination of the peak values in the adjacent registers so as to reduce power dissipation, a case beyond the total limit of length of the maximum scan chain also being taken into consideration so that the registers must be arranged to shorten the scan chain on the occasion; and

(c) $L_{lim}>L^{max}$: at the time of arrangement of the scan chain registers at a next step, the total limit of length of the maximum scan chain not being taken into consideration

but a search for a set of peak values in the adjacent registers to reduce power dissipation; wherein i stands for any of the registers, and the distance D_i^{min} indicates the distance of a register i closer to the other registers, the distance D_i^{max} indicates the distance of a register i further from the other registers, and the distance D_i^{avg} indicates the distance of a register i equidistant from the other registers are estimated, namely $L^{min}=\Sigma_i D_i^{min}$, $L^{max}=\Sigma_i D_i^{max}$, and $L^{avg}=\Sigma_i D_i^{avg}$.

Claim 2 (currently amended): The method as claimed in claim 1, wherein ~~steps of~~ creating the database of the two adjacent registers includes:

(a) dividing **[[the]]** distributed areas on **[[the]]** coordinates of all registers into **[[the]]** **a** form of grids, and storing a grid attributed to each register;

(b) recording a register falling in each grid; and

(c) searching for **and recording** a group of the two adjacent registers according to the maximum **of connection** distance ~~limit~~ in the grid and in **[[the]]** **a** circumference of the grid~~, and then recording them~~.

Claim 3 (currently amended): The method as claimed in claim 1, wherein **[[an]]** **the** event ~~impossibly~~ meeting both the maximum **of the connection length and the maximum** limited distance **of connection** is ~~deleted~~ **ignored** in **[[the]]** case of**:**

(a) existence in a register without any corresponding group of the two adjacent registers **which indicates** ~~: indicating~~ that the design is provided with no feasible solution;

(b) existence in a register with only an adjacent register **which indicates** ~~: indicating~~ that the register must be the output terminal of the scan chain, and **[[its]]** **the** adjacent register is second in arrangement order;

(c) existence in two registers with only an adjacent register:

i. both of the two adjacent registers~~: indicating~~ **which indicates** that no feasible solution is given; and

ii. two registers different from each other~~: indicating~~ **which indicates** that one register can be made to be **[[the]]** **an** input terminal of the scan chain, and the other, to be **[[the]]** **an** output terminal; and

(d) at least four registers with only an adjacent register~~: indicating~~ **which indicates** that no feasible solution is given.

Claim 4 (canceled).

Claim 5 (currently amended): The method of reordering a scan chain for the design of testability on VLSI with low power dissipation as claimed in claim **[[1]]** **3**, wherein **the** scan chain registers are reordered to**:**

(a) decide a next optimal register to be arranged; and

(b) decide an optimal register of the output terminal.

Claim 6. The method of reordering a scan chain for the design of testability on VLSI with low power dissipation as claimed in claim 5, **further comprising:** ~~**wherein in order to decide a next optimal register to be arranged, the algorithm tool according to this invention uses**~~

using a logical XOR calculation **[[to]]** every time **to** sort out a next optimal register in a set of registers having not been arranged in the course of arrangement so that the opposite test patterns can be little different from the test patterns of registers so far having been arranged, thereby reducing the probability of register state conversion in each shift.

Claim 7 (original): The method of reordering a scan chain for the design of testability on VLSI with low power dissipation as claimed in claim 3, wherein in order to decide an optimal register of the output terminal after the scan chain registers reordered includes:

(a) the special case of the built database of registers adjacent to each other occurs when (1) a register **exists** ~~**is existed**~~ with an adjacent register only; and (2) two registers **exist** ~~**are existed**~~ respectively with an adjacent register only, and the two registers are different from their adjacent registers;

(b) when no special cases occur, the minority of adjacent registers among all registers is used as the registers at the output; and

(c) when a database of registers adjacent to each other is provided, of all registers, a register of maximum power dissipation is used as **[[an]]** **the** output terminal, and that less different from the test pattern is used as **[[an]]** **the** input terminal.